WHAT IS CLAIMED IS:

1. A semiconductor chip comprising:

a semiconductor substrate;

a first active region disposed in the substrate;

a second active region disposed in the substrate;

a resistor formed in the first active region, the resistor including a doped region formed between two terminals; and

a strained channel transistor formed in the second active region, the strained channel transistor including first and second stressors formed in the substrate oppositely adjacent a strained channel region.

2. The chip of claim 1 wherein the channel region comprises a first semiconductor material having a first natural lattice constant and the first and second stressors each comprise a second semiconductor material having a second natural lattice constant that is different than the first natural lattice constant.

3. The chip of claim 2 wherein the second natural lattice constant is larger than the first natural lattice constant.

4. The chip of claim 2 wherein the first semiconductor material comprises silicon and the second semiconductor material comprises silicon and germanium.

5. The chip of claim 4 wherein the transistor is a p-channel transistor.

6. The chip of claim 2 wherein the second natural lattice constant is smaller than the first natural lattice constant.

7. The chip of claim 2 wherein the first semiconductor material is silicon and the second semiconductor material comprises silicon and carbon.

8. The chip of claim 7 wherein the transistor is an n-channel transistor.

9. The chip of claim 1 wherein the doped region has a doping type that is opposite to a doping type of a portion of the semiconductor substrate underlying the doped region.

10. The chip of claim 1 wherein the doped region has a doping concentration in the range of about $10^{16}$ to about $10^{19}$ $cm^{-3}$.

11. The chip of claim 1 wherein the doped region has a n-type doping.

12. The chip of claim 1 wherein the doped region has a p-type doping.

13. The chip of claim 1 wherein the transistor further comprises a gate dielectric overlying the channel region, the gate dielectric comprising a high permittivity dielectric selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthanum oxide, cerium oxide, titanium oxide, tantalum oxide, and combinations thereof.

14. The chip of claim 13 wherein the transistor further comprises a gate electrode overlying the gate dielectric, the gate electrode is formed from a material selected from the group

consisting of poly-crystalline silicon, poly-crystalline silicon-germanium, a metal, a metallic nitride, a metallic silicide, a metallic oxide, and combinations thereof.

15. The chip of claim 1 wherein the semiconductor substrate comprises a bulk semiconductor substrate.

16. The chip of claim 1 wherein the semiconductor substrate comprises a semiconductor-on-insulator substrate.

17. A method of forming a semiconductor chip, the method comprising:

providing a semiconductor region comprising a first semiconductor material with a first natural lattice constant;

forming first and second active regions in the semiconductor region;

forming a gate stack over the second active region;

forming a masking layer over the first active region;

after forming the masking layer, forming at least one recess in a portion of the second active region not covered by the gate stack;

growing a second semiconductor material in the at least one recess, the second semiconductor material having a second natural lattice constant that is different than the first natural lattice constant;

forming source and drain regions in the second active region to form a strained channel transistor;

removing the masking layer; and

forming a semiconductor component in the first active region.

18. The method of claim 17 wherein the step of forming first and second active regions comprises the steps of:

forming trenches to define the active regions;

filling the trenches with a trench filling material; and

doping the active regions.

19. The method of claim 17 wherein forming the second semiconductor material comprises performing a chemical vapor deposition step.

20. The method of claim 17 wherein forming the second semiconductor material comprises performing a selective epitaxy step.

21. The method of claim 17 wherein forming a semiconductor component comprises forming a doped region in the first active region to form a resistor.

22. The method of claim 21, further comprising forming at least two electrical contacts that are electrically coupled to the doped region.

23. The method of claim 21 wherein forming the doped region comprises performing an ion implantation step.

24. The method of claim 17 wherein forming the source and drain regions comprises performing an ion implantation step.

25. The method of claim 17 and further comprising forming a cap layer overlying the second semiconductor material, the cap layer comprising the first semiconductor material.

26. The method of claim 17 wherein the gate stack comprises a gate electrode overlying a gate dielectric.

27. The method of claim 26 wherein the gate stack further comprises a gate mask overlying the gate electrode.

28. The method of claim 17 wherein the second natural lattice constant is larger than the first natural lattice constant.

29. The method of claim 17 wherein the first semiconductor material comprises silicon and the second semiconductor material comprises silicon and germanium.

30. The method of claim 29 wherein forming source and drain regions comprises P-typed doped regions.

31. The method of claim 17 wherein the second natural lattice constant is smaller than the first natural lattice constant.

32. The method of claim 17 wherein the first semiconductor material is silicon and the second semiconductor material comprises silicon and carbon.

33. The method of claim 17 further comprising a step of forming silicide on the gate stack, the source region, and the drain region of the strained channel transistor.

34. The method of claim 17 further comprising steps of:

forming contact etch stop layer over the resistor and the semiconductor component;

forming passivation layer over the contact etch stop layer; and

forming contacts to the resistor and transistor through the contact etch stop layer.

35. The method of claim 17 wherein the semiconductor component comprises a transistor.

36. The method of claim 35 wherein the transistor comprises a strained channel field effect transistor.

37. The method of claim 35 wherein the strained channel transistor comprises a transistor of first doping type and wherein the semiconductor component comprises a transistor of a second doping type.

38. The method of claim 35 and further comprising:

forming a disposable film over the second active region, the disposable film overlying the gate stack; and

processing the disposable film to form disposable spacers on sidewalls of the gate stack in the second active region;

wherein the at least one recess is formed adjacent a disposable spacer.

39. The method of claim 38 and further comprising removing the disposable spacers, and forming spacers on the sidewalls of gate stack.

40. The method of claim 35 and further comprising forming a second gate stack over the first active region, wherein the first gate stack and second gate stack each comprises a gate electrode overlying a gate dielectric.

41. The method of claim 17 and further comprising a hard mask overlying the gate electrode and spacers.

42. The method of claim 41 wherein the hard mask comprises multiple layers of material.

43. The method of claim 41 and further comprising, after growing the second semiconductor material, removing the hard mask.

44. The method of claim 17 wherein the second semiconductor material is in-situ doped with a p-type dopant.

45. The method of claim 44 wherein the second semiconductor material is in-situ doped with a dopant selected from the group consisting of boron, indium, and combinations thereof.

46. The method of claim 17 wherein the second semiconductor material is in-situ doped with an n-type dopant.

47. The method of claim 46 wherein the second semiconductor material is in-situ doped with a dopant selected from the group consisting of As, P, Sb, and combinations thereof.

48. The method of claim 17 and further comprising, after forming the source and drain regions, forming a first conductive material on the source and drain regions.

49. The method of claim 48 wherein the first conductive material comprises cobalt germanosilicide Co(SiGe), nickel germanosilicide Ni(SiGe), Co(SiC), or Ni(SiC), or combinations thereof.

50. A method of forming a semiconductor device, the method comprising:

providing a semiconductor substrate comprising a first semiconductor material, the substrate including a first active region and a second active region, the first active region having a first gate stack formed thereon and the second active region having a second gate stack formed thereon;

forming a film over first active region and second active region;

forming spacers on sidewalls of the second gate stack in the second active region;

etching a source recess and a drain recess on opposing sides of the second gate stack, the source recess and the drain recess spaced from a channel region by the spacers; and

growing a second semiconductor material in the source recess and the drain recess.

51. The method of claim 50 wherein the first gate stack and second gate stack each comprise a gate electrode overlying a gate dielectric.

52. The method of claim 51 further comprising a hard mask overlying the gate electrode and spacers.

53. The method of claim 52 wherein the hard mask comprises multiple layers of hard mask material.

54. The method of claim 52 wherein the hard mask comprises silicon oxide, silicon oxynitride, silicon nitride, or combinations thereof.

55. The method of claim 52 and further comprising, after growing the second semiconductor material, removing the hard mask.

56. The method of claim 50 wherein the first semiconductor material comprises silicon.

57. The method of claim 56 wherein the second semiconductor material comprises silicon and germanium.

58. The method of claim 56 wherein the second semiconductor material comprises silicon and carbon.

59. The method of claim 50 wherein the semiconductor substrate comprises an insulator layer underlying the first semiconductor material.

60. The method of claim 50 wherein the semiconductor substrate comprises a relaxed SiGe layer underlying the first semiconductor material.

61. The method of claim 60 wherein the first semiconductor material comprises silicon.

62. The method of claim 50 wherein the second semiconductor material is in-situ doped with a p-type dopant.

63. The method of claim 62 wherein the p-type dopant is selected from the group consisting of boron, indium, and combinations thereof.

64. The method of claim 50 wherein the second semiconductor material is in-situ doped with an n-type dopant.

65. The method of claim 64 wherein the n-type dopant is selected from the group consisting of As, P, Sb, and combinations thereof.

66. The method of claim 50 and further comprising:

forming a first source region and a first drain region in the first active region oppositely adjacent to the first gate stack; and

forming a second source region and a second drain region in the second active region oppositely adjacent to the second gate stack.

67. The method of claim 66 and further comprising, after forming the first source region and the first drain region, forming a first conductive material on the first source region and the first drain region.

68. The method of claim 67 wherein the first conductive material comprises cobalt silicide CoSi, nickel silicide NiSi, cobalt germanosilicide Co(SiGe), nickel germanosilicide Ni(SiGe), Co(SiC), Ni(SiC) or combinations thereof.

69. The method of claim 66 and further comprising, after forming the second source region and the second drain region, forming a second conductive material on the second source region and the second drain region.

70. The method of claim 69 wherein the second conductive material comprises cobalt silicide CoSi, nickel silicide NiSi, cobaltgermanosilicide Co(SiGe), nickelgermanosilicide Ni(SiGe), Co(SiC), Ni(SiC) or combinations thereof.

71. The method of claim 50 wherein forming spacers on sidewalls of the second gate stack comprises:

forming a disposable film over the second active region including the second gate stack;

and

forming disposable spacers by etching the disposable film.

72. The method of claim 71 wherein the step of forming a film over the first active region and the second active region comprises the step of forming a disposable film, the method further comprising forming a masking layer over a portion of the disposable film overlying the first active region prior to forming disposable spacers.

73. The method of claim 71 wherein forming disposable spacers comprises performing a plasma etch process or a wet etch process.

74. The method of claim 71 and further comprising removing the disposable spacers after forming the source recess and the drain recess.

75. The method of claim 74 and further comprising, after growing the second semiconductor material, forming spacers on sidewalls of the first gate stack and the second gate stack.

76. The method of claim 75 wherein the spacers on the sides of first and second gate stacks are composite spacers.

77. The method of claim 50 wherein growing a second semiconductor material comprises a performing selective epitaxy process.

78. The method of claim 50 and further comprising, after growing a second semiconductor material, selectively growing a first semiconductor material overlying the second semiconductor material.

79. The method of claim 50 wherein the first gate stack and the second gate stack each include a gate electrode formed from a material selected from the group consisting of polycrystalline silicon, polycrystalline silicon-germanium, a metal, a metal silicide, a metal nitride, and combinations thereof.

80. The method of claim 50 wherein the first gate stack and the second gate stack each include a gate dielectric formed from a material selected from the group consisting of silicon oxide, silicon oxynitride, silicon nitride, hafnium oxide, aluminum oxide, zirconium oxide, or combinations thereof.

81. A method of forming a semiconductor device, the method comprising;

providing a semiconductor layer that includes a first active region and a second active region;

forming a first gate stack over the first active region and a second gate stack over the second active region;

forming a dielectric film over the first active region and the second active region;

forming a masking layer over a portion of the dielectric film overlying the second active region;

forming disposable spacers on sidewalls of the first gate stack by anisotropically etching the dielectric film;

forming first and second recesses in the first active region substantially aligned with the disposable spacer;

filling the first and second recesses with a semiconductor material; and

implanting source and drain regions in the second active region adjacent the second gate stack.

82. The method of claim 81 and further comprising, after filling the first and second recesses, removing the disposable spacers and the dielectric film over the first active region.

83. The method of claim 82 and, after removing the disposable spacers and the dielectric film, further comprising:

forming lightly doped regions of a first conductivity type in the first active region adjacent the first gate stack;

forming lightly doped regions of a second conductivity type in the second active region adjacent the second gate stack;

forming first spacers adjacent the first gate stack and second spacers adjacent the second stack;

forming heavily doped regions of the first conductivity type in the first active region adjacent the first spacers; and

forming heavily doped regions of the second conductivity type in the first active region adjacent the first gate stack.

84. The method of claim 81 and, after filling the first and second recesses, further comprising:

removing the masking layer from over the second active region;

forming a second masking layer over the first active region; and

etching the dielectric layer over the second active region to form second spacers adjacent the second gate stack.

85. The method of claim 84 wherein implanting a source region and a drain region comprises implanting a source region and a drain region in the second active region aligned with the second spacers.

86. The method of claim 85 and further comprising, after implanting the source region and the drain region, removing the disposable spacers and the second spacers.

87. The method of claim 86 and further comprising, after removing the disposable spacers and the second spacers, forming a first lightly doped region in the first active region adjacent the first gate stack and forming a second lightly doped region in the second active region adjacent the second gate stack.